

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		<i>Complete if Known</i> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Application Number</td> <td colspan="4">09/551027</td> </tr> <tr> <td>Filing Date</td> <td colspan="4">April 17, 2000</td> </tr> <tr> <td>First Named Inventor</td> <td colspan="4">Noble Jr., Wendell</td> </tr> <tr> <td>Group Art Unit</td> <td colspan="4">2822</td> </tr> <tr> <td>Examiner Name</td> <td colspan="4">Trinh, Michael</td> </tr> </table>					Application Number	09/551027				Filing Date	April 17, 2000				First Named Inventor	Noble Jr., Wendell				Group Art Unit	2822				Examiner Name	Trinh, Michael			
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US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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MT	JP-2000-164883	06/16/2000	Yamazaki, S., et al	H01L	29/786	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS							
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					T ²
MT		RHYNE, In: <u>Fundamentals of Digital Systems Design</u> , Prentice Hall, New Jersey, (1973), pg. 70-71					
MT		SU, D., et al. "Experimental Results and Modeling Techniques for Substrate Noise in Mixed Signal Integrated Circuits", <u>IEEE Journal of Solid State Circuits</u> , 28(4), (1993), pp. 420-430					

EXAMINER

Michael Trinh

DATE CONSIDERED

9/16/02